ELC 441
DIGITAL ENGINEERING SYSTEMS
(1.0 CU - 3 lecture hours, 1 design hour)

Course Information **Professor: Orlando Hernandez**
Fall 2016: MW 5:30PM–6:50PM/7:00PM-7:25PM/AR148

Course Description: A treatment of digital system engineering problems: power, noise, signaling, and timing.

Instructor Information:
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Office Hours:
Tuesdays 11:00 AM - 12:20 PM
Thursdays 2:00 PM – 3:20 PM
By appointment (send me email)
And whenever my office door is open

Textbook: *Digital Systems Engineering*, by William J. Dally and John W. Poulton, CAMBRIDGE UNIVERSITY PRESS, 2008.
ISBN 978-0521-06175-9

Corequisite: Digital Circuits and Microprocessors (ENG 312) and Electronics (ELC 251)

Grading Policy:

Homework	10%
Homework will be announced for each chapter after the chapter has been covered.	
Midterm Exam	30%
Comprehensive Final Exam	40%
Design Projects	20% (Projects 1 and 2: 5% each, Project 3: 10%)

Tips for Success:
Read the book sections prior to their discussion in class.
Do as much homework as possible. Attempt to do all the problems, even the ones that have not been assigned.
Do not be shy about asking questions, either during class or outside of the class.

College Level Policies:
Attendance Policy: http://www.tcnj.edu/~recreg/policies/attendance.html

Academic Integrity Policy: http://www.tcnj.edu/~academic/policy/integrity.html

Americans with Disabilities Act (ADA) Policy: http://www.tcnj.edu/~affirm/ada.html

Tentative Agenda:

Week	Topics	Reading
1 Monday 8/29	**INTRODUCTION TO DIGITAL SYSTEMS ENGINEERING** Why Study Digital Systems Engineering? And Engineering View of a Digital System Technology Trends and Digital Systems Engineering **PROJECT ORIENTATION AND LECTURE**	CHAPTER 1.1 – 1.3

Tentative Agenda (continued):

Week	Topics	Reading
2, 3	**PACKAGING OF DIGITAL SYSTEMS**	
Monday 9/5	A Typical Digital System	CHAPTER 2.1 – 2.8
Monday 9/12	Digital Integrated Circuits – On-Chip Wiring	
	Integrated Circuits Packages	
	Printed Circuit Boards	
	Chassis and Cabinets	
	Backplane and Motherboards	
	Wire and Cable	
	Connectors	
	PROJECT 1: Introduction to HyperLynx and the DSA8300 Digital Serial Analyzer	
4, 5	**MODELING AND ANALYSIS OF WIRES**	
Monday 9/19	Geometry and Electrical Properties	CHAPTER 3.1 – 3.7
Monday 9/26	Electrical Models of Wires	
	Simple Transmission Lines	
	Special Transmission Lines	
	Wire Cost Models	
	Measurement Techniques	
	Some Experimental Measurements	
	Signal Integrity and Time Domain Reflectometry (TDR) Basics	
	PROJECT 1: Introduction to HyperLynx and the DSA8300 Digital Serial Analyzer	
6, 7	**POWER DISTRIBUTION**	
Monday 10/3	The Power Supply Network	CHAPTER 5.1 – 5.6
Monday 10/10	Local Regulation	
	Logic Loads and On-Chip Power Supply Distribution	
	Power Supply Isolation	
	Bypass Capacitors	
	Example Power Distribution System	
	PROJECT 2: HyperLynx Simulations	
8, 9	**MIDTERM**	
Monday 10/17	**NOISE IN DIGITAL SYSTEMS**	
Monday 10/24	Noise Sources in a Digital System	CHAPTER 6.1 – 6.6
	Cross Talk	
	Intersymbol Interference	
	Other Noise Sources	
	Managing Noise	
	PROJECT 2: HyperLynx Simulations	
10, 11	**SIGNALING CONVENTIONS**	
Monday 10/31	A Comparison of Two Transmission Systems	CHAPTER 7.1 – 7.4
Monday 11/7	Considerations in Transmission System Design	
	Signaling Modes for Transmission Lines	
	Signaling Over Lumped Transmission Media	
	PROJECT 3: HyperLynx Simulations and TDR Measurements	
12	**ADVANCED SIGNALING TECHNIQUES**	
Monday 11/14	Signaling Over RC Interconnect	CHAPTER 8.1 – 8.5
	Driving Lossy LC Lines	
	Simultaneous Bidirectional Signaling	
	AC and N of M Balanced Signaling	
	Examples	
	PROJECT 3: HyperLynx Simulations and TDR Measurements	

Tentative Agenda (continued):

Week	Topics	Reading
13, 14	**TIMING CONVENTIONS**	
Monday 11/21	A Comparison of Two Timing Conventions	CHAPTER 9.1 – 9.3
Monday 11/28	Considerations in Timing Design	
	Timing Fundamentals	
	Open-Loop Synchronous Timing	CHAPTER 9.5 – 9.7
	Closed-Loop Timing	
	Clock Distribution	
	PROJECT 3: HyperLynx Simulations and TDR Measurements	
15	**SYNCHRONIZATION**	
Monday 12/5	A Comparison of Three Synchronization Strategies	CHAPTER 10.1 – 10.3
	Synchronization Fundamentals	
	Synchronizer Design	
	PROJECT 3: HyperLynx Simulations and TDR Measurements	
16	**COMPREHENSIVE FINAL EXAM**	
Monday 12/12		

Educational Objectives

(What TCNJ ECE engineers should be able to accomplish during the first few years after graduation)

The Department of Electrical and Computer Engineering at the College of New Jersey seeks to prepare its graduates:

- To contribute to the economic development of New Jersey and the nation through the ethical practice of engineering;
- To become successful in their chosen career path, whether it is in the practice of engineering, in advanced studies in engineering or science, or in other complementary disciplines;
- To assume leadership roles in industry or public service through engineering ability; and
- To maintain career skills through life-long learning.

Electrical and Computer Engineering Student Outcomes

(What TCNJ Electrical and Computer Engineering students are expected to know and be able to do at graduation. What knowledge, abilities, tools and skills the programs give the graduates to enable them to accomplish the Educational Objectives)

The Student Outcomes listed below are expected of all graduates of the Electrical or Computer Engineering Program.

ECE graduates will have:

a. an ability to apply knowledge of mathematics, science and engineering;
Students use mathematical and physics concepts as tools to analyze issues of signaling, power, and noise in high speed digital systems. The use these tools in homework problems, projects, and exams.

b. an ability to design and conduct experiments, as well as to analyze and interpret data;

c. an ability to design a system, component, or process to meet desired needs;
Students perform projects that involve design.

d. an ability to function in multidisciplinary teams;

e. an ability to identify, formulate and solve engineering problems;
Students perform projects that involve the solution of engineering problems.

f. an understanding of professional and ethical responsibility;

g. an ability to communicate effectively;
Students write three Project Reports.

h. the broad education necessary to understand the impact of engineering solutions in a global and societal context;

i. a recognition of the need for and an ability to engage in life-long learning;

j. a knowledge of contemporary issues;

k. an ability to use the techniques, skills and modern engineering tools necessary for engineering practice;
Students use state of the art Time Domain Reflectometry (TDR) equipment and software to perform measurements and design involving TDR techniques.

Course Objectives:*

Objective 1 To understand the design issues in high performance digital systems. [a, c, e, m]

Objective 2 To model of the underlying physical and electrical mechanism of power distribution, information signaling, and system timing in high speed digital systems. [a, c, e, g, k]

Objective 3 To use these model to find engineering design solutions to noise, signaling, timing and power distributions problems of high performance digital systems. [a, c, e, g, k]

Topics Covered:

1. High-speed engineering models for wires
2. Power distribution in digital systems
3. Noise Management
4. Signaling methods for high performance systems
5. Timing and synchronization

Evaluation:

A. Comprehensive Final
B. Midterm Exam
C. Homework
D. Project Report

Performance Criteria:**

Objective 1

a. The student will be able to explain and deal with the issues of noise, signaling, timing, and power distribution in high performance digital systems. [A, B, C, D]
b. The student will be able to correlate the effect to these issues on system performance. [A, B, C, D]

Objective 2

a. The student will be able to model wires as either lumped elements or transmission lines depending upon their function, length and operating frequency for a particular application. [A, B, C, D]
b. The student will be able to model power distribution systems with either a DC or an AC supply current for high-speed systems. [A, B, C, D]
c. The student will be able to identify, model, and control the different noise sources, including skew and jitter, that impact the signaling and timing performance of digital systems. [A, B, C, D]

Objective 3

a. The student will be able to determine the appropriate wire model, both on-chip and off-chip, appropriate for a particular high-speed digital system design. [A, B, C, D]
b. The student will be able to minimize power distribution problems in the design of high performance digital systems. [A, B, C, D]
c. The student will be able to manage the different noise sources, including skew and jitter, to meet high performance system requirements. [A, B, C, D]

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* Small letters in brackets refer to the Program Outcomes
** Capital letters in brackets refer to the evaluation methods used to assess student performance